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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CEHIC, KENAN	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,526	WEGO ET AL.	
	Examiner	Art Unit	
	Kenan Cehic	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/02/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 03/02/2005 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

2. The abstract of the disclosure is objected to because of "disclosed" in line 2. Correction is required. See MPEP § 608.01(b).

Applicant is reminded of the proper language and format for an abstract of the disclosure.

3. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the counter in claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Claim Objections

6. Claim 10-18 are objected to because of the following informalities:

For claim 10, the claim limitation "the associated data buffer", in line 8 is the first occurrence. It is suggested to applicant to change this to –an associated data buffer--. Similar problems exist in line 13.

For claim 12, claim limitation "each entry" in line 2 seems to refer back to "each entry" in claim 10 line 7. If this is true, it is suggested to change this limitation to –said each entry--. Similar problems exist in claim 16 line 2.

For claim 13, the claim limitation "the same frame" in line 2, is the first occurrence. It is suggested to applicant to change this limitation to –a same frame--. Similar problems exist in claim 17 and 18 line 2.

For claim 14, claim limitation "time-slot buses" in line 6 seems to refer back to "time-slot buses" in line 2. If this is true, it is suggested to change this limitation to –said time-slot buses --.

For claim 14, claim limitation "an output line" in line 10 seems to refer back to "an output line" in line 6. If this is true, it is suggested to change this limitation to –said output line --.

For claim 15, the claim limitation "the first entry" in line 4, is the first occurrence. It is suggested to applicant to change this limitation to –a first entry--.

For claim 15, the claim limitation "the entry" in line 6, is the first occurrence. It is suggested to applicant to change this limitation to –an entry--.

For claim 15, the claim limitation "the associated output line" in line 7, is the first occurrence. It is suggested to applicant to change this limitation to –an associated output line --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 11 recites the limitation "the data buffer" in line 3. There is insufficient antecedent basis for this limitation in the claim.

It is not clear which data buffer the applicant is referring to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 14, 15 rejected under 35 U.S.C. 102(b) as being anticipated by McHarg et al. (US 5,291,482).

For claim 14, McHarg discloses A communication network node (see Figure 2 "Fast Packet switch"), said node (see Figure 2 "Fast Packet switch") comprising:

one or more time slot slot (see column 5 lines 21-30 "time multiplexed" and column 8 lines 27-35 "time slots") buses (see Figure 2, 212 and column 5 lines 21-30 and "read bus") operative to transfer (see column 2 lines 48-51 "throughput of data") frames (see

column 8 lines 27-32 "frames" , "frame" and column 7 lines 48-50 "each frame") from a plurality of serial (see Figure 5 "Serial Link Data Input")

input lines (see column 5 lines 21-23 "input ports" and Figure 2 "Incoming Ports")

located on a receiving side (see column 5 lines 21-23 "channel come into ...switch through ....input ports") of the node (see Figure 2 "Fast Packet switch") to a plurality of serial (see Figure 10 "Serial Link Data Output") output lines (see Figure 2, "Outgoing Ports") located on the transmitting side (see Figure 2 "Outgoing Ports") of the node (see Figure 2 "Fast Packet switch");

one data buffers (see Figure 2, 200) for each time-slot (see column 5 lines 26-27 "time multiplexed" and column 8 lines 27-35 "time slots") bus (see Figure 2, 210 and column 5 lines 26-29 "write bus") at the transmitting side (see Figure 2 "Outgoing Ports" and 204 are transmitters) operative

to buffer (see column 5 lines "write received packet data into buffer") the frames (see column 8 lines 27-32 "frames" , "frame" and column 7 lines 48-50 "each frame") from time-slot (see column 5 lines 26-27 "time multiplexed" and column 8 lines 27-35 "time slots") buses (see Figure 2, 210 and column 5 lines 26-29 "write bus") before forwarding transmission (see column 5 lines 39-42 "read data from buffer...transmit packets to the circuit switching fabric") to an output line (see Figure 2, "Outgoing Ports"); and,

a connection table (see column 5 lines 8-12 "TX pointer FIFO queue" and column 6 lines 22-23 "lookup table"), wherein each entry (see column 6 lines 34-36 "pointers") in the connection table (see column 5 lines 8-12 "TX pointer FIFO queue" and column 6 lines

22-23 "lookup table") contains at least a data address pointing (see column 6 lines 39-44 "pointer"; pointer is also an address) to a byte (see column 6 lines 42-44 "addresses in buffer" and column 11 lines 42-45 "buffer location address"; any address in a memory is part of some byte) in one of the data buffers buffer (see Figure 2, 200 and column 63-66 "packet buffer 200"), and wherein the entries (see column 6 lines 34-36 "pointers") are arranged in the same order (see column 6 lines 32-36 "FIFO") as their corresponding bytes (see column 6 lines 42-44 "addresses in buffer" and column 11 lines 42-45 "buffer location address"; any address in a memory is part of some byte) are to be transferred (see column 6 lines 34-47 "FIFO" and "buffer 200 from which to read")to an output line (see column 5 lines 39-42 "transmit packets...through output ports")

For claim 15, McHarg disclose one starting pointer (column 13 lines 62-66 "5-bit PUSH pointer") per output line (see column 13 lines 59-62 "XMTR pointer FIFOs, one for each packet channel" and column 6 lines 34-41 "Each packet transmitter queries ...FIFO associated with its packet channels") is allocated to one memory area (see column 6 lines 27-32 "one FIFO for each packet channel") in the
connection table (see column 6 lines 27-32 "XMTR pointer FIFO") for each of the output lines (see column 6 lines 37-39 "Each packet transmitter" and column 11 lines 5-8 "packet transmitter...for each ....channels...on an output port") and points to the first entry (see column 14 lines 1-6 "lower address bits") in each memory
area (see column 14 lines 4-6 "appropriate XMTR pointer FIFO"); and,

one indexing pointer (column 13 lines 62-66 "5-bit POP pointer") per output line (see column 13 lines 59-62 "XMTR pointer FIFOs, one for each packet channel" and column 6 lines 34-41 "Each packet transmitter queries ...FIFO associated with its packet channels") points at the entry (see column 14 lines 17-21 an lines 32-36 "POP is pending"; pop pointer is pointing to a location into FIFO that holds the next pointer) in the connection table (see column 6 lines 27-32 "XMTR pointer FIFO") holding the address (see column 14 lines 17-20 "pointer") to the byte (see column 6 lines 42-44 "addresses in buffer" and column 11 lines 42-45 "buffer location address"; any address in a memory is part of some byte) currently being fetched (see column 14 lines 33-37 "read by transmitter" and column 6 lines 37-44 "address in buffer 200 from which to read") from one of the buffers (see column 6 lines 37-44 "address in buffer 200 from which to read") to the associated output line (see column 13 lines 59-62 "XMTR pointer FIFOs, one for each packet channel" and column 6 lines 34-41 "Each packet transmitter queries ...FIFO associated with its packet channels").

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claim 10,11 are rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg et al. (US 5,291,482) in view of Cui et al (US 6,625,234 A1), hereinafter McHarg and Cui.

Regarding claim 1, McHarg disclose a communication network node (see Figure 2 "Fast Packet switch"), said node (see Figure 2 "Fast Packet switch") comprising:

one or more time slot (see column 5 lines 21-30 "time multiplexed" and column 8 lines 27-35 "time slots") buses (see Figure 2, 212 and column 5 lines 21-30 and "read bus") operative to transfer (see column 2 lines 48-51 "throughput of data") frames (see column 8 lines 27-32 "frames" , "frame" and column 7 lines 48-50 "each frame") from a plurality

of serial (see Figure 5 "Serial Link Data Input") input lines (see column 5 lines 21-23 "input ports" and Figure 2 "Incoming Ports")

located on a receiving side (see column 5 lines 21-23 "channel come into ...switch through ....input ports") of the node (see Figure 2 "Fast Packet switch") to a plurality of serial (see Figure 10 "Serial Link Data Output") output lines (see Figure 2, "Outgoing Ports") located on the transmitting side (see Figure 2 "Outgoing Ports") of the node (see Figure 2 "Fast Packet switch"),

one data buffers (see Figure 2, 200) at the receiving side (see Figure 2, 200 receives data from write bus 210 and column 4 lines 56-62 "receivers that have access to buffer 200") of each time-slot (see column 5 lines 26-27 "time multiplexed" and column 8 lines 27-35 "time slots") bus (see Figure 2, 212 and column 5 lines 21-30 "read bus"), operative to buffer (see column 5 lines 26-34 "read from buffer") the frames (see column 8 lines 27-32 "frames" , "frame" and column 7 lines 48-50 "each frame") from the input lines see column 5 lines 21-23 "input ports" and Figure 2 "Incoming Ports")

before transmission (see column 5 lines 39-42 "read data from buffer...transmit packets to the circuit switching fabric");

a connection table (see column 5 lines 8-12 "TX pointer FIFO queue" and column 6 lines 22-23 "lookup table") for each time-slot (see column 5 lines 26-27 "time multiplexed" and column 8 lines 27-35 "time slots") bus (see Figure 2, 212 and column 5 lines 21-30 "read bus"), wherein each entry (see column 6 lines 34-36 "pointers") in the connection table (see column 5 lines 8-12 "TX pointer FIFO queue" and column 6 lines 22-23 "lookup table") contains at least a data address pointing (see column 6 lines 39-44

"pointer"; pointer is also an address) to a byte (see column 6 lines 42-44 "addresses in buffer" and column 11 lines 42-45 "buffer location address"; any address in a memory is part of some byte) in the associated data buffer (see Figure 2, 200 and column 63-66 "packet buffer 200"),

and wherein the entries (see column 6 lines 34-36 "pointers") are arranged in the same order (see column 6 lines 32-36 "FIFO") as their corresponding bytes (column 11 lines 42-45 "buffer location address"; any address in a memory is part of some byte)

are to be transferred (see column 6 lines 34-47 "FIFO" and "buffer 200 from which to read") on a data bus (see column 5 lines 39-42 "read bus 212"); and

a clock (see column 11 lines 15-17 "system clock") used (see figure 10 ,1000 and 212, packet transmitter access buffer via multiplexed read buffer 212) by the time-slot (see column 5 lines 26-27 "time multiplexed" and column 8 lines 27-35 "time slots"; column 7 lines 14-17 "time slot") bus (see Figure 2, 212 and column 5 lines 21-30 "read bus") for transmission of time slots (see column 5 lines 26-27 "time multiplexed" and column 8 lines 27-35 "time slots"; column 7 lines 14-17 "time slot") bus (see Figure 2, 212 and column 5 lines 21-30 "read bus"),

McHarg is silent about: as regarding claim 1, a counter, synchronized to a clock, said counter operative to indicate which byte in the associated data buffer that presently is to be read out from the data-bus buffer into a time slot in the associated data bus by indexing the entries of the connection table.

Cui from the same or similar field of endeavor teaches a counter (see Figure 6, 650), synchronized (see column 2 lines 37-38 "clock to synchronize the data with a counter")

to a clock (see Figure 6, 670), said counter (see Figure 6, 650) operative to indicate (see column 6 lines 28-36 "the pointer to each block is the output of the table lookup N1 630 and a two-stage counter 640, 650") which byte (see column 6 lines 28-36 "pointer to each block") in the associated data buffer (see Figure 6, 610) that presently is to be read out (see column 6 lines 25-27 "read out from the working memory to the buffer memory) from the data-bus (see Figure 6 "Data bus") buffer (see Figure 6, 610) into a time slot (see column 5 lines 16-19 "rate of data retrieved from memory") in the associated data bus (see Figure 6 "Data bus") by indexing (see column 6 lines 33-36 "table lookup...controlled by the N1 counter 650) the entries (see column 2 lines 25-17 "addresses") of the connection table (see Figure 6, 630) .

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of McHarg et al. by using the features, as taught by Cui et al., in order to provide ... (see column 2 lines 15-18).

13. Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg et al. (US 5,291,482) in view of Cui et al (US 6,625,234 A1) as applied to claim 10 above, and further in view of Blanc et al (US 6,728,251).

McHarg and Cui et al teach the claimed invention as described in paragraph 11.

McHarg and Cui et al are silent about: wherein each entry in the connection table contains, in addition to the data address, a control field.

Blanc et al from the same or similar field of endeavor teaches a switching apparatus with the following features:

Blanc et al wherein each entry (see column 7 lines 43-45 "control word") in the connection table (see column 7 lines 43-45 "OUT_mapping table") contains, in addition to the data address (see column 7 lines 45-49 "OFFSET field"), a control field (see column 7 lines 45-49 "control field").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of McHarg et al. in view of Cui et al by using the features, as taught by Blanc et al ,in order to provide ... (see column 2 lines 37-42).

14. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg et al. (US 5,291,482) in view of Cui et al (US 6,625,234 A1) as applied to claim 10 above, and further in view of Loge et al. (US 2003/0076780 A1).

For claim 13, McHarg and Cui teach the claimed invention as described in paragraph 11.

McHarg and Cui additionally, as regarding claim 13, disclose wherein there is only one data buffer (see column 2 lines 48-51 " one buffer") for each time slot (see column 5 lines 21-30 "time multiplexed" and column 8 lines 27-35 "time slots") bus (see Figure 2, 212 and column 5 lines 21-30 and "read bus") .

McHarg and Cui is silent about :as regarding claim 13, within the same frame, a data location in the buffer is not read before write-in.

Loge et al from the same or similar field of endeavor teaches a packet switching part with the features:

within the same frame (see section 0079 lines 2-8 "periodic frame"),a data location (see section 0079 lines 2-8 "banks of registers of the buffer memory") in the buffer (see section 0079 lines 2-8 "buffer memory") is not read (see section 0079 lines 2-8 "periodic frame for write access") before write-in (see section 0079 lines 2-8 "periodic frame for read access").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of McHarg et al. in view of Cui et al by using the features, as taught by Loge et al.,in order to provide ... (see section 0026).

15. Claim 16 rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg et al. (US 5,291,482) in view of Blanc et al (US 6,728,251).

McHarg teach the claimed invention as described in paragraph 8.

McHarg is silent about: wherein each entry in the connection table contains, in addition to the data address, a control field.

Blanc et al from the same or similar field of endeavor teaches a switching apparatus with the following features:

Blanc et al wherein each entry (see column 7 lines 43-45 "control word") in the connection table (see column 7 lines 43-45 "OUT_mapping table") contains, in addition to the data address (see column 7 lines 45-49 "OFFSET field"), a control field (see column 7 lines 45-49 "control field").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of McHarg et al. by using the features, as taught by Blanc et al ,in order to provide ... (see column 2 lines 37-42).

16. Claim 17, 18 rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg et al. (US 5,291,482) in view of Loge et al. (US 2003/0076780 A1).

For claim 17, 18, McHarg and Cui teach the claimed invention as described in paragraph 8.

McHarg additionally, as regarding claim 13, disclose wherein there is only one data buffer (see column 2 lines 48-51 " one buffer") for each time slot (see column 5 lines 21-30 "time multiplexed" and column 8 lines 27-35 "time slots") bus (see Figure 2, 212 and column 5 lines 21-30 and "read bus") .

McHarg is silent about :as regarding claim 13, within the same frame,

a data location in the buffer is not read before write-in.

Loge et al from the same or similar field of endeavor teaches a packet switching part with the features:

within the same frame (see section 0079 lines 2-8 "periodic frame"),a data location (see section 0079 lines 2-8 "banks of registers of the buffer memory") in the buffer (see section 0079 lines 2-8 "buffer memory") is not read (see section 0079 lines 2-8 "periodic frame for write access") before write-in (see section 0079 lines 2-8 "periodic frame for read access").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of McHarg by using the features, as taught by Loge et al.,in order to provide ... (see section 0026).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US-4,791,629 A	12-1988	Burns et al.
US-5,172,376 A	12-1992	Chopping et al.
US-5,495,478 A	02-1996	Wilkinson et al.
US-2005/0175025 A1	08-2005	Beadle et al.
US-7,110,359 B1	09-2006	Acharya, Yatin R.
US-7,126,946 B2	10-2006	Beadle et al.
US-7,190,696 B1	03-2007	Manur et al.

The above are recited to show switching/buffering methods.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenan Cehic whose telephone number is (571) 270-3120. The examiner can normally be reached on Monday through Friday 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KC

KWANG BIN YAO
SUPERVISORY PATENT EXAMINER